WHAT IS CLAIMED IS:

1. An output buffer, comprising:
   a first circuit coupled between a first power line and a pad; and
   a second circuit coupled between a second power line and the pad, comprising:
   a resistor constructed by a well region of a second conductivity type deposited on a substrate of a first conductivity type, the resistor comprising a first end and a second end, the first end being a doped region of the second conductivity type at least partially overlapping the well region and coupled to the pad;
   a first doped region of the first conductivity type, electrically floated in the well region; and
   an electrostatic discharge protection component, coupled between the second end and the second power line.

2. The output buffer of claim 1, wherein the second circuit further comprises a capacitor coupled between the pad and the first doped region.

3. The output buffer of claim 1, wherein the electrostatic discharge protection element is a MOS transistor comprising a gate, a drain and a source, the drain being coupled to the second end of the resistor 0 and the source being coupled to the second power line.

4. The output buffer of claim 3, wherein the drain and the source are respectively comprised of a second doped region of the second conductivity type and a third doped region of the second conductivity type.

5. The output buffer of claim 3, wherein the gate is coupled to a signal source.

6. The output buffer of claim 3, wherein the gate is coupled to the second power line.

7. The output buffer of claim 3, wherein the MOS transistor is a finger-shaped MOS.

8. The output buffer of claim 1, wherein the first and the second ends are respectively comprised of a fourth doped region of the second conductivity type and a fifth doped region of the second conductivity type.

9. The output buffer of claim 8, wherein the first doped region is deposited between the fourth doped region and the fifth doped region.

10. The output buffer of claim 8, wherein the electrostatic discharge protection component is a MOS transistor of the second conductivity type, the MOS transistor being comprised of a gate, a drain, a source, and a substrate, the drain being composed of the fifth doping region and the source being coupled to the second power line.

11. The output buffer of claim 8, wherein the first doping region interlaces with the fourth doped region.

12. The output buffer of claim 8, wherein the first doped region is in contact with the fourth doped region.

13. The output buffer of claim 1, wherein, during an ESD event, the first doped region is coupled to the first end.

14. The output buffer of claim 1, wherein the substrate is coupled to the second power line through the sixth doped region.

15. An electrostatic discharge protection circuit, coupled between a first pad and a second pad, comprising:

a resistor consisted of a well region of a second conductivity type, deposited on the substrate of a first conductivity type, and coupled to the first pad;

a first doped region of the first conductivity type, electrically floated in the well region; and

a electrostatic discharge protection component, coupled between the well region and the second pad.

16. The electrostatic discharge protection circuit of claim 15, wherein, during an ESD event, the first doped region is coupled to the first pad.

17. The electrostatic discharge protection circuit of claim 15, wherein the first pad is coupled to an output port and the second pad is coupled to a power line.

18. The electrostatic discharge protection circuit of claim 15, wherein the first and the second pads are respectively coupled to a first and a second power lines.

19. The electrostatic discharge protection circuit of claim 15, wherein the electrostatic discharge protection component is a MOS transistor of the second conductivity

type, the MOS transistor comprising a gate, a drain, a source and a substrate, the drain being coupled to the resistor and the source being coupled to the second pad.

20. The electrostatic discharge protection circuit of claim 19, wherein the gate is coupled to the second pad.

21. The electrostatic discharge protection circuit of claim 19, further comprising a delaying circuit which consists of a resistor and a capacitor connected in series, the delaying circuit being coupled between the first pad and the second pad, the gate being coupled to a node for connecting the resistor and the capacitor.

22. The electrostatic discharge protection circuit of claim 19, wherein the drain is coupled to a first pad.

23. The electrostatic discharge protection circuit of claim 15, wherein the electrostatic discharge protection component is a field oxide device.

24. The electrostatic discharge protection circuit of claim 23, wherein the field oxide device comprises a second doped region of the second conductivity type and a third doped region of the second conductivity type, the second doped region and the third doped region being formed on the substrate.

25. The electrostatic discharge protection circuit of claim 24, wherein the field oxide device further comprises a field oxide layer formed between the second and the third doped regions.

26. The electrostatic discharge protection circuit of claim 15, wherein the substrate is coupled to the second

pad via a sixth doped region of the first conductivity type.

27. The electrostatic discharge protection circuit of claim 26, wherein the sixth doped region partly embraces the electrostatic discharge protection circuit.

28. The electrostatic discharge protection circuit of claim 26, wherein a seventh doped region of the second conductivity type is formed between the sixth doped region and the well region.

29. The electrostatic discharge protection circuit of claim 15, wherein the first conductivity type is n-type and the second conductivity type is p-type.

30. The electrostatic discharge protection circuit of claim 15, wherein the first conductivity type is a p-type and the second conductivity type is an n-type.

31. An output buffer, comprising:

a first circuit, coupled between a first power line and a pad; and

a second circuit coupled between a second power line and a pad, comprising:

a resistor, comprised of a well region of the second conductivity type and comprising a first end and a second end, the first end being a doped region of a second conductivity type overlapping the well region and coupled to the pad;

a first doped region of the first conductivity type, electrically floating in the well region; and

an electrostatic discharge protection component, coupled between the second end and the second power line.

32. An electrostatic discharge protection circuit, coupled between a first pad and a second pad, comprising :

a resistor, which consists of a second well region of a second conductivity type and coupled to the first pad;

a first doped region of a first conductivity type, electrically floated in the second well region; and

a electrostatic discharge protection component, deposited on a first well region of a first conductivity type and coupled between the second well region and the second pad.

33. The electrostatic discharge protection circuit of claim 32, further comprising a first capacitor coupled between the first pad and the first doped region.